WHAT IS CLAIMED IS:

1. An integrated circuit device having a plurality of input terminals, comprising:

a plurality of input buffers provided to the plurality of input terminals;

a plurality of serial parallel conversion circuits for converting, in serial-parallel, outputs of the input buffers, respectively; and

a plurality of boundary scan registers which input selectively an output of the input buffer or an input of a test data, holds the input data, and outputs selectively the held input data or an output of the serial parallel conversion circuit,

wherein the plurality of boundary scan registers are connected serially to constitute a shift register.

2. The integrated circuit device according to claim 1, wherein the boundary scan register comprises:

a first selector circuit for selectively inputting the output of the input buffer or the input of the test data; and

a second selector circuit for selectively outputting the held input data or the output of the serial parallel conversion circuit.

3. The integrated circuit device according to claim 2, wherein the serial parallel conversion circuit has a plurality

of outputs, and the second selector circuits are provided in correspondence to the plurality of outputs of the serial parallel conversion circuit.

4. The integrated circuit device according to claim 1, wherein the input terminals include differential input terminal pairs for inputting differential inputs, respectively, and the input buffer receives the differential input, and outputs an input of the serial parallel conversion circuit.

5. An integrated circuit device having a plurality of output terminals, comprising:

a plurality of parallel serial conversion circuits for converting, in parallel-serial, an internal signal;

a plurality of output buffers which are provided to the plurality of output terminals, and to which an output of the parallel serial conversion circuit is supplied; and

a plurality of boundary scan registers which selectively input the internal signal or an input of a test data, hold the input data, and selectively output the held input data or an output of the output buffer,

wherein the plurality of boundary scan registers are serially connected to constitute a shift register.

6. The integrated circuit device according to claim 5, wherein the boundary scan register comprises:

a first selector circuit for selectively inputting the

internal signal or the input of the test data; and

a second selector circuit for selectively outputting the held input data or the output of the output buffer.

7. The integrated circuit device according to claim 6, wherein the output buffer outputs a differential output, and the second selector circuit selectively outputs a complementary signal of the held input data or the differential output of the output buffer.

8. The integrated circuit device according to claim 6, wherein a plurality of the internal signals are input into the parallel serial conversion circuit, and an AND signal, OR signal, or an exclusive OR signal of the plurality of internal signals are input to the first selector circuit as the internal signal.

9. An integrated circuit device having a plurality of output terminals, comprising:

a plurality of parallel serial conversion circuits for converting, in parallel-serial, an internal signal;

a plurality of output buffers which are provided to the plurality of output terminals, and to which an output of the parallel serial conversion circuit is supplied;

a plurality of boundary scan registers which selectively input the internal signal or an input of the test data, hold the input data, and selectively output the held input data

or an output of the parallel serial conversion circuit,

wherein the plurality of boundary scan registers are serially connected to constitute a shift register.

10. The integrated circuit device according to claim 9, wherein the boundary scan register comprises:

a first selector circuit for selectively inputting the internal signal or the input of the test data; and

a second selector circuit for selectively outputting the held input data or the output of the parallel serial conversion circuit.